IN THE CLAIMS:

1. An integrated circuit comprising:

a lower metal interconnect layer located over a semiconductor body;

a multi-level dielectric layer located over said lower interconnect layer;

an upper metal interconnect layer located over said multi-level dielectric layer; and

a thin film resistor located within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer.

2. The integrated circuit of claim 1, further comprising:

a first plurality of conductively filled vias extending from said upper metal interconnect layer to said lower interconnect layer; and

a second plurality of conductively filled vias extending from said upper metal layer to said thin film resistor.

3. The integrated circuit of claim 1, wherein said thin film resistor comprises a hard mask located over an end of the thin film resistor.

4. The integrated circuit of claim 3, wherein said hard mask comprises TiW.

5. The integrated circuit of claim 3, wherein said hard mask comprises TiN.

6. The integrated circuit of claim 1, wherein said thin film resistor comprises TaN.

7. The integrated circuit of claim 1, wherein said thin film resistor comprises SiCr.

8. The integrated circuit of claim 1, wherein said thin film resistor comprises NiCr.

9. A method of fabricating an integrated circuit, comprising the steps of:

forming a first metal interconnect layer over a semiconductor body;

forming a first dielectric over said first metal interconnect layer;

forming a thin film resistor over said first dielectric;

forming a second dielectric over said first dielectric and said thin film resistor; and

forming a second metal interconnect layer over said second dielectric.

10. The method of claim 9, further comprising the step of forming vias in said first dielectric and said second dielectric to said first interconnect layer and in said first dielectric to said thin film resistor.

11. The method of claim 9, wherein the step of forming said thin film resistor comprises the steps of:

depositing a layer of resistor material over said first dielectric;

depositing a hard mask layer over said layer of resistor material;

forming a first pattern over said hard mask where said thin film resistor is desired;

etching said hard mask and said layer of resistor material to form said thin film resistor; and

removing at least a portion of said hard mask.

12. The method of claim 11, wherein said step of removing at least a portion of said hard mask comprises the steps of:

forming a second pattern over said hard mask, said pattern covering the ends of said thin film resistor; and

etching said hard mask with a solution of hydrogen peroxide.

13. The method of claim 11, wherein said step of removing at least a portion of said hard mask comprises the step of removing all of said hard mask with a solution of hydrogen peroxide.

14. The method of claim 11, wherein said hard mask comprises TiW.

15. The method of claim 11, wherein said hard mask comprises TiN.

16. The method of claim 9, further comprising the steps of:

measuring a distance from a top of a silicon substrate in said semiconductor body to a top of said first dielectric; and

adding a third dielectric over said first dielectric prior to depositing said layer of resistor material such that said distance plus a thickness of said third dielectric is approximately equal to an odd integer number of laser quarter wavelengths.

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